Single-Wire Bus – Simple, Practical, Viable

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A single-wire or 1-wire data bus is a serial data bus. Its architecture comprises a master that communicates with one or more slaves. Data exchange can do without a separate clock line if the master is taking care of data line timing. This structure lends itself for applications that feature relatively time-uncritical communication tasks such as sensor readout, actuator control, or saving measurement data or parameters that have to be available on demand.

The bus can exchange data in two directions; it can however only operate in half-duplex mode. Data transmission is performed at a data rate of 15kbits/sec in standard speed or 111kbits/sec in Overdrive mode (see fig. 1). Since a total of just two lines is needed for data communication and powering of the network devices, network partners can perform their functions in a remote configuration via cables. In particular, this eases reading out sensor signals and saves costs because low-cost cabling can be used. Of course, any possible influence of nearby, strong interference fields needs to be analyzed beforehand. Due to its fairly low data transfer or bit rate, the bus itself will hardly emit any interference.

Figure 1

The single-wire bus originally dates back to by Dallas / Maxim. These companies had intended to design a link which would both provide a power and communication link using just one line. The bus is laid out for 5V and 3V designs, but ICs are already available for 1.8V. Naturally, the line in its idle mode will always be in a logic state of "1" since the supply voltage is connected to the data bus. In its simplest case, this is done by a 1 to 5 kÙ pull-up resistor, which is connected between the data line and supply voltage, and by using open-drain stages in the outputs of all devices that are connected to the bus. Data communication, however, requires that the voltage of the communication line will temporarily be pulled down to ground. Consequently, slave circuits need to contain a sufficiently large capacitor to maintain the slave's supply voltage, and this capacitor is often integrated in the corresponding device. Inherently, such a structure cannot transmit unlimited amounts of power, so that the connected circuitry needs to be designed for lowest possible power consumption. As a consequence, loads driven by actuators need to be powered separately. Due to the buffer capacitors, the recovery time (the time required for a signal level to change from "0" to "1") will be variable. This recovery time is a function of the number of slaves connected to the bus. The more slaves, and the longer the cable / PCB conductor, the longer will be the recovery time that is dependent on the increasing capacitance to ground and respectively on the increasing series resistance. Consequently, the effective data rate will be lower, both in standard speed and in overdrive mode. The effect of line loading is particularly apparent in overdrive mode. However, the decrease in data rate or the increase in recovery time is also influenced by the system voltage and the expected operating temperature.

Recent experiments have shown that under favourable conditions, line length can be extended to a maximum of 300 meters with fully functional and error free data transmission. In this experiment, 30 network participants with varying functions were connected on the end of the line. A 1kΩ resistor was used as pull-up, and the bus was controlled using an 8051-compatible μC made by Maxim. Using a communications port adapter, the majority of available PCs were able to operate with a bus length of 200m. It is advisable to keep line capacitance as low as possible. Recommended cable characteristics are less or equal than 15pF/m, as is specified for twisted pair cabling.

In many applications, network participants (slaves) can be used with self-sufficient power like a dedicated power supply, a battery or solar cells etc. Naturally, by using these measures, the data line is subject to a lower load, and any effects on the data rate due to the recovery time will be considerably reduced. Also, using a buffer capacitor can be avoided. The lower load on the data line also has a positive effect on the maximum usable line length.

Another feature of the single-line system is that the slave ICs are delivered with a uniquely defined 64-bit address (ID). This ID is issued centrally for all components, so that device addresses are unique all over the world and cannot be manipulated. In other words, Maxim has marked every single IC with a unique ID during final test. This allows to uniquely access any end product that is equipped with a single-wire IC, no matter in which network the network participant with that ID will show up – it will always have the same address. Due to its unique ID, application/board/IC traceability can be provided easily.

These features open up highly interesting applications in the areas of access control or management of serial numbers. Software versions can safely be identified, and any recorded operation data can clearly be assigned. Using an additional SHA-1 encryption, a safeguarded data transmission (protected against improper use) can be performed in environments that need to be protected. This e.g. applies to FPGA programming data, or to the detection of components that are not authorized to intervene in a system, to read data or to change parameters (see figures 2 and 3).

A typical application for such a bus is the 'i-Button' system, which is easy to set up, with a rugged mechanic and works reliably. This structure allows for the construction of small, robust and low-cost temperature and humidity data loggers, or of authentification systems

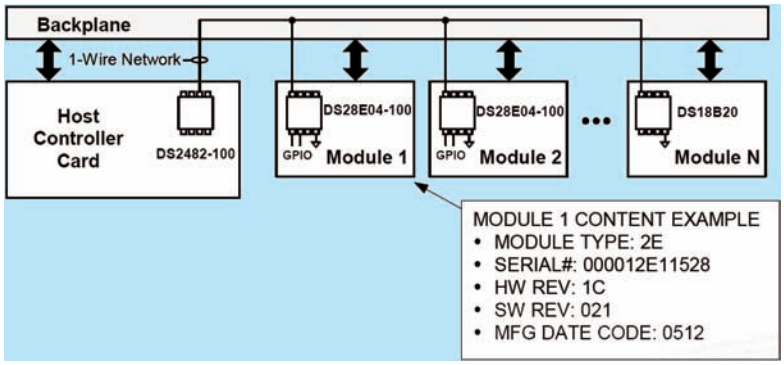

Figure 2

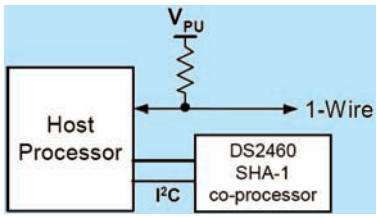

Figure 3

for access and user privilege control, which can be combined with biometric data for even higher security.

A number of products are available that can be used directly in single-wire environments:

- Single-wire interface products such as USB-to-single-wire or I2C-to-single-wire bridges, which act as a master on the single-wire bus. These products contain firmware for their master function as well as line drivers and/or level shifters. In turn, such an interface circuit can be controlled by any microcontroller. The line driver uses a forced pull-up to ensure that more power can be driven across the bus or that longer lines can be controlled.
- Memory such as EPROM, SRAM, EEPROM, ROM or NV SRAM. These devices act as self-contained memory on the bus, and also have their own, fixed ID burnt into a separate on-board ROM.
- Temperature sensors and temperature switches with resolutions of up to 12 bits, accuracies down to 0.5°C, an operating temperature range of -55 to +125°C and adjustable switching thresholds that can be preserved even after powering down the system.
- A four-channel A/D converter that works with up to 16 bits resolution and a sampling rate of 1k samples/s.
- Real-time clocks which are available as simple RTC or as data recorder with integrated RTC.
- Battery management ICs and protection circuits which monitor charging status, temperature, over- and undervoltage as well as overcurrent and short-circuit conditions. All of these circuits are designed to monitor Li-Ion batteries - some of them additionally support NiMH batteries. The circuits help to provide the best charging method for any given battery type: A connected charger unit can be identified via the data line, and charging operation can be enabled only after a parameter match has been detected (or after the required parameters have been transmitted to the charger controller). If the ID is missing because some other product was connected, then charging operation is automatically disabled.

No matter which function out of the elements mentioned above is concerned, every IC will have a unique 64-bit ID that consists of three sections: 8 bits of CRC, a 48 bits wide serial number and 8 bits for a group affiliation. Any specific single-wire bus participant is identified using a 'process of elimination', in which the bus master reads out the addresses bit by bit after initialization.

Even if the master does not know the serial numbers (IDs) of the units connected to the bus, it still can access any specific unit, send configuration data and read out measurement data using the ReadROM, MatchROM and SearchROM commands. The latter works like the ReadROM command in connection with MatchROM. After an initialization via reset and issuing the SearchROM command, all units on the bus will simultaneously return the logic value of the first ROM bit (LSB) in two consecutive read cycles. During these two read cycles, the slaves will first output the non-inverted and then the inverted values, which will all be read by the master. The logic operation on the bus is an 'AND' because the bus uses pull-up stages, and because the participants need to actively pull the data line to ground.

If all connected participants contain a "0" at this address position, then a value of 01 is passed back to the master. This is because a "0" will be on the bus in the first run, and then a "1" as inverted value in the second run. If all participants have a "1" in this location, then in analogy, a value of 1" will be read back, because a "1" will be on the bus first (no slave is pulling the level down), and then a "0" as inverted value. If the addresses on this position contain both "0" and "1", then the answer will be 00, which points to a conflict, because the AND function only requires one single participant to have a "0" transmitted on the bus. An answer of 11 is the last possibility. However, this answer is irrelevant since it only indicates that no participants are connected to the bus. In case of a conflict, the master will transmit a "0" to select all participants whose values are "0" in this address location. From this point onward, all other participants will remain inactive until a reset pulse is sent on the bus. Subsequently, the procedure is repeated for the next more significant bit. If during a query step all participants happen to have a "0" or "1", then the master will write a "0" or "1" (depending on the value found) before it moves on to the next bit. After this first selection step, 63 further read/selection cycles will be executed until only one participant will remain, so that the unit's address has been fully detected. This means that every selection step consists of two read and one write cycle, or two read time slots and one write time slot. If there is more than one participant connected to the network, then the controller will continue by determining the next address, initiating another search sequence. Then, the controller will send a "1" instead of a "0" for the address bit location with the highest significance that exhibited a conflict. This disables the address branch that has already been identified. The next search run for the detection of the third address will begin at the conflict location with the second-highest bit significance. This sequence continues until all participants have been detected.

Apart from the required CPU time, this entire learning and addressing process will take approximately 13.16 milliseconds. Thus, 75 participants can be identified and addressed per second in normal speed mode.

As is customary for modern designs, single-wire evaluation kits are available for faster familiarization and as reference examples. Moreover, Maxim provides a wide choice of application reports. These range from a comparative overview of serial busses to layout guidelines and suggested software design solutions.Ω